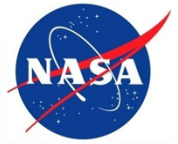

15th Annual Components for Military and Space Electronics (CMSE) Conference

Class Y – Non-hermetic ICs for Space

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Background

- Military standards for microcircuits haven't kept pace with developments in packaging technology
  - RADC (Rome Air Development Center) used to be the technical arm of DLA (Defense Logistic Agency) and they did necessary evaluations to keep up with new developments. But they are long gone.
- Existing set of 38535 Classes N, Q and V no longer adequate to cover new complex microcircuits such as the Xilinx Virtex-4 FPGAs.
- NEPAG (NASA EEE Parts Assurance Group), which is like a large component engineering group representing space agencies, is addressing these issues:

Some NEPAG Activities:

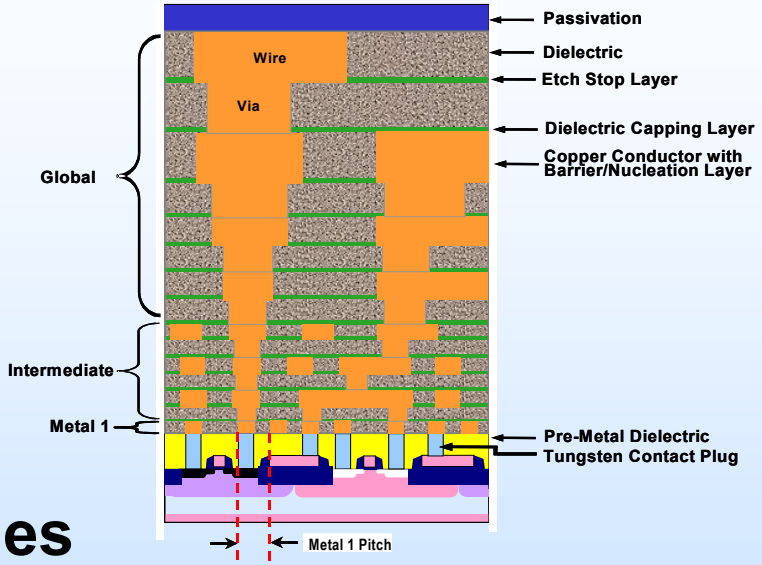
- Weekly telecons
- Supplier audit
- DLA Land & maritime SMD review
- Others

Background (Cont'd)

- NEPAG (NASA EEE Parts Assurance Group), which is like a large component engineering group representing space agencies, is addressing these issues: (Cont'd)
  - 38535 Appendix H, new technology evaluation, was completely revised. This effort was led by Larry Harzstark.
  - Requirement for screening of passive elements, used in IC packages for signal integrity, was added to 38535.
  - An out-of-box approach was taken to address non-hermetic parts, e.g., V-4; concept of a new class (termed Class Y) was developed by Mike Sampson.
  - A G-12 Task Group was formed in January 2010. It is led by the NASA/JPL team of Shri Agarwal, Ramin Roosta and Tom Wilson.

Outline

- What is Electronic Packaging?
- Why Package Electronic Parts?
- Evolution of Packaging
- New Application Challenges and Solutions
- Associated Assurance Challenges
- The Class Y Concept and Possible Extensions
- Embedded Technologies
- NEPP Activities

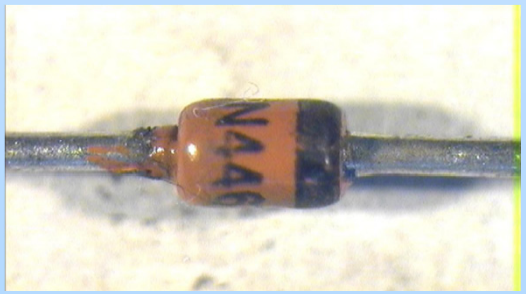


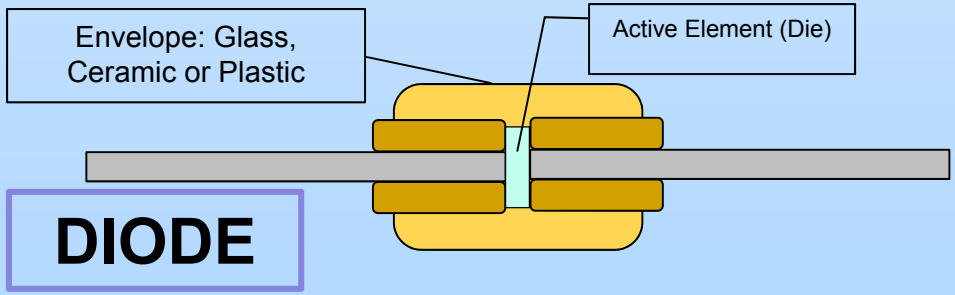
What is Electronic Packaging?

- Electronic “Packaging” can have two basic meanings:
  - First (Part) Level: The “envelope” of protection surrounding an active electronic element, and also the termination system to connect it to the outside world
  - Second and Higher Levels: The assembly of parts to boards, boards to slices, slices to boxes, boxes to systems, instruments and spacecraft
- This discussion covers examples of both

Why Package Electronic Parts?

- To protect the active element against:
  - Handling
  - Shock and vibration
  - Contamination
  - Light penetration or emission
- To provide a suitable system to make connection between the element and the printed wiring board
- To prevent conductive parts of the element from coming in contact with other conductive surfaces, unless intended





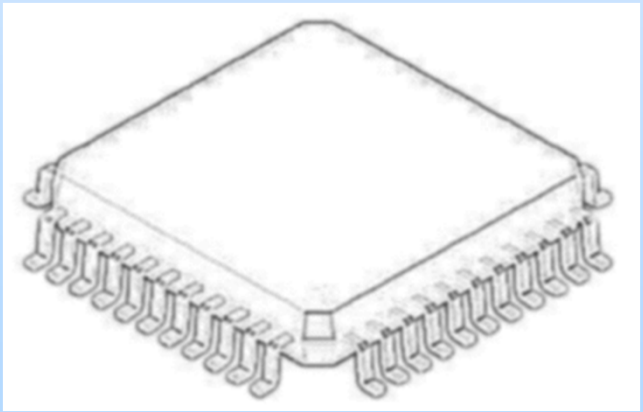
Package Options – Hermetic?

- Once, hermetic packages were the preferred option
- Now, few hermetic options for latest package technologies
  - Development of new hermetic options unattractive
    - Very high Non Recurring Expenses
    - Very high technical difficulty
    - Very low volume
    - Demanding customers
- Market is driven by consumer products
  - Low cost
  - High volume
  - Rapid turnover
  - "Green"
  - Minimized size

  = Non hermetic, mostly plastic
- New hermetic technologies may become available but timing is uncertain

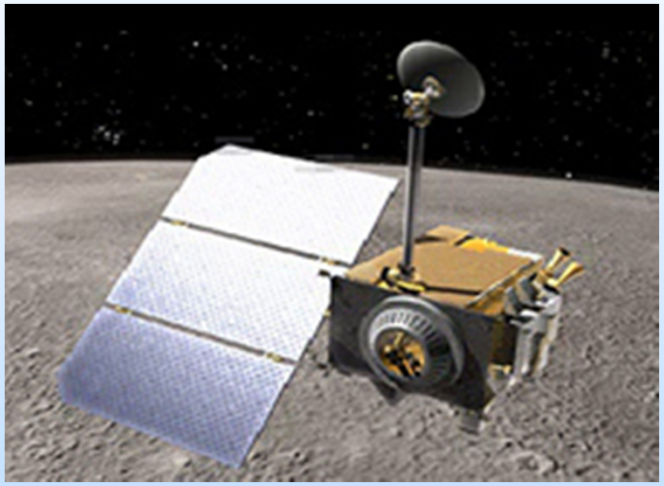
The “General” Package

- **Typically, packages consist of the same basic features but achieve them in many ways:**
  - **Functional elements - active die, passives etc.**
  - **Interconnects between elements (2 or more elements)**
  - **A substrate**
  - **Interconnects to the external I/O of the package**
  - **A protective package**
  - **Interconnects to the next higher level of assembly**



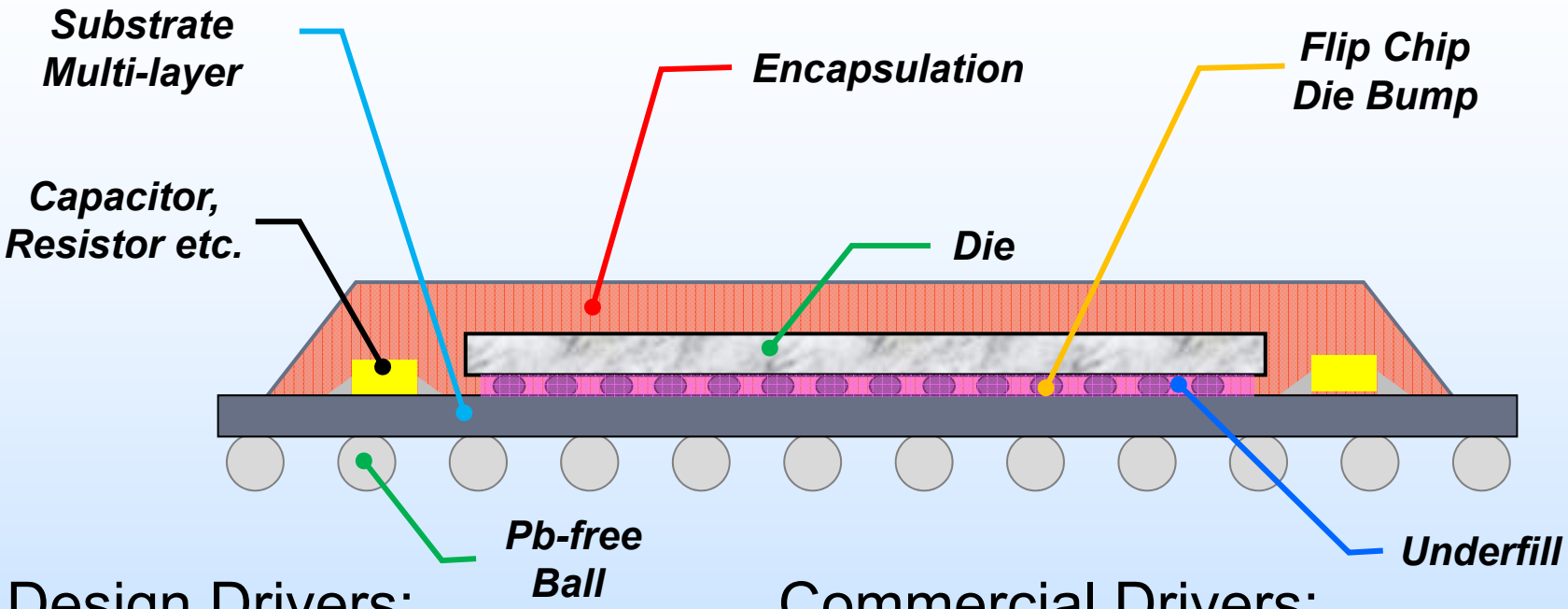
Continuous Packaging Challenges

- I/O s, increasing number, decreasing pitch
- Heat Dissipation, (especially in space)
- Manufacturability
- Materials
- Mechanical
- Installation
- Testability
- Inspectability
- RoHS (Pb-free)
- (Space Environment)



Lunar Reconnaissance Orbiter (LRO), Built at GSFC, Launched with LCROSS, June 18,2009

Commercial, Non-hermetic Package (PBGA*)



Design Drivers:

- High I/O count
- Large die
- Environmental protection
- Performance/Speed
- Ancillary parts

Commercial Drivers:

- Low cost
- High volume
- Limited life
- Automated installation
- Compact

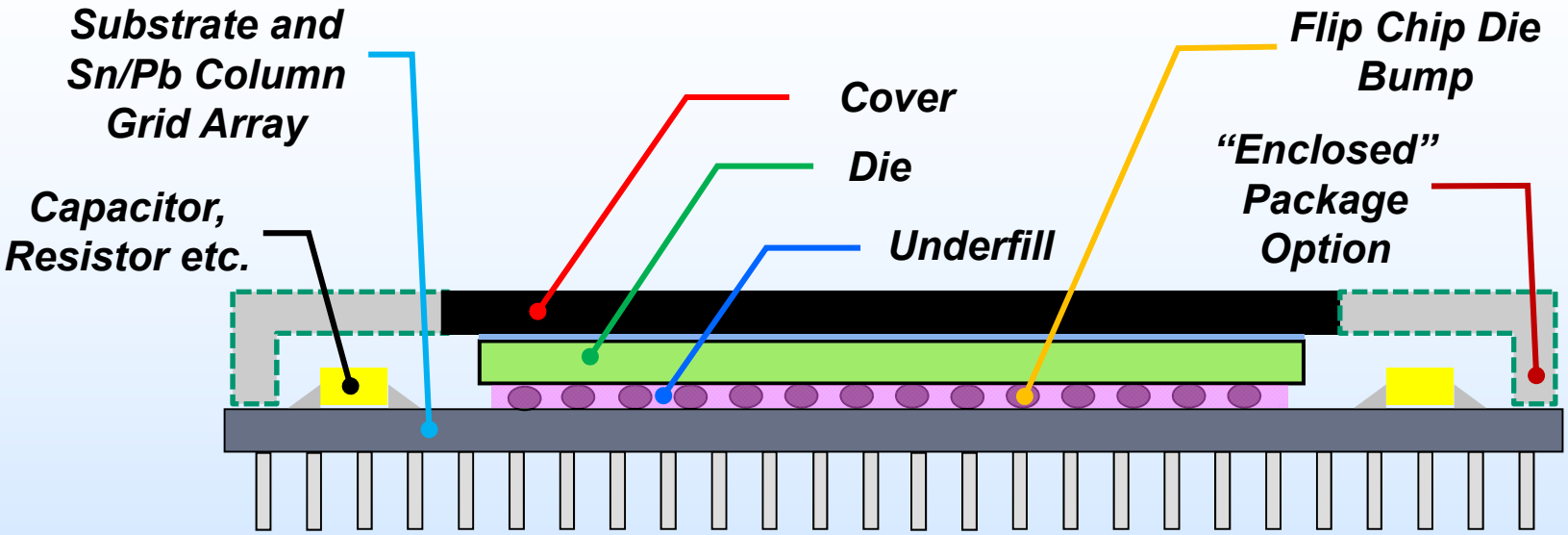
* PBGA: Plastic Ball Grid Array

Space Challenges for Complex Non-hermetic Packages

- **Vacuum:**
  - Outgassing, offgassing, property deterioration
- **Foreign Object Debris (FOD)**
  - From the package threat to the system, or a threat to the package
- **Shock and vibration**
  - During launch, deployments and operation
- **Thermal cycl**ing
  - Usually small range; high number of cycles in Low Earth Orbit (LEO)
- **Thermal management**
  - Only conduction and radiation transfer heat
- **Thousands of interconnects**
  - Opportunities for opens, intermittent - possibly latent
- **Low volume assembly**
  - Limited automation, lots of rework
- **Long life**
  - Costs for space are high, make the most of the investment
- **Novel hardware**
  - Lots of “one offs”
- **Rigorous test and inspection**
  - To try to find the latent threats to reliability

ONE STRIKE AND YOU’RE OUT!

Non-hermetic Package, With"Space" Features (CCGA*?)



Space Challenge	Some Defenses
Vacuum	Low out/off-gassing materials. Ceramics vs polymers.
Shock and vibration	Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer
Thermal cycling	Compliant/robust interconnects, matched thermal expansion coefficients
Thermal management	Heat spreader in the lid and/or substrate, thermally conductive materials
Thousands of interconnects	Process control, planarity, solderability, substrate design
Low volume assembly	Remains a challenge
Long life	Good design, materials, parts and process control
Novel hardware	Test, test, test
Rigorous test and inspection	Testability and inspectability will always be challenges

* Ceramic Column Grid Array

Hermeticity

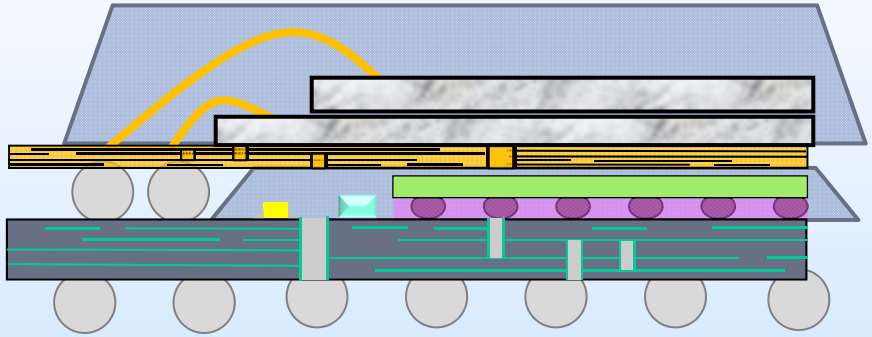
- **NASA prefers hermetic packages for critical applications**
- **Hermeticity is measureable, assuring package integrity**
- **Only 3 tests provide assurance for hermetic package integrity:**
  - **Hermeticity – nothing bad can get in**
  - **Residual or Internal gas analysis – nothing bad is inside**
  - **Particle Impact Noise Detection – no FOD inside**
- **NON-HERMETIC PACKAGE INTEGRITY IS HARD TO ASSESS - NO 3 BASIC TESTS**
- **Non-hermetic packages expose materials' interfaces that are locked away in hermetic ones**

But What is Hermetic?

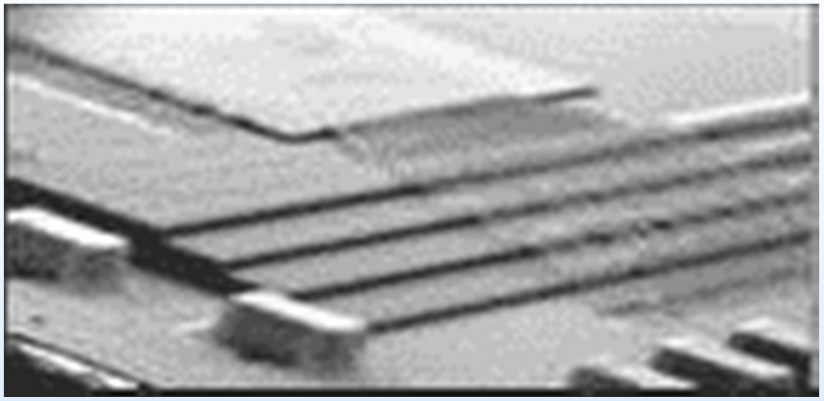
- **Per MIL-PRF-38534 Appx E and 38535 Appx A, hermetic packages must consist of metals, ceramic and glass in combinations ONLY, no polymerics**
- **Meets aggressive leak rate test limits**
  - **Verifies low rate of gas escape/ atmospheric interchange**
  - **Even so, small volume packages meeting "tight limits" theoretically exchange their atmosphere very quickly:**
    - **0.001 cc, exchanges 93% in 1 month at $5X10^{-8}$ atmosphere/cc/sec!**
    - **1.0cc, 96% in 10 years at $1 X 10^{-8}$**
  - **Even large packages with quite small leaks can surprise**
    - **10 cc, 96% in 1 year at $1 X 10^{-6}$!**
- **For applications in space vacuum why care?**
  - **Risk for contamination on the ground**
  - **Risk for outgassing in vacuum**

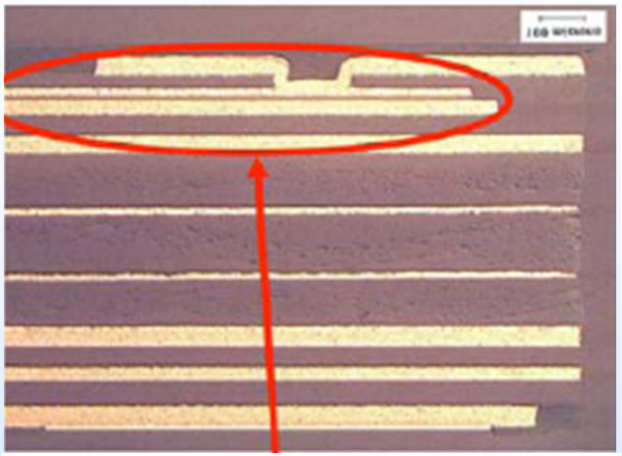
Non-hermetic Package Variations

- Current and future package options mix and match elements in almost infinite combinations
- Elements include:
  - Wire bonds
  - Ball interconnects
  - Solder joints
  - Conductive epoxies
  - Vias
  - Multi-layer substrates
  - Multiple chips, active and passive (hybrid?)
  - Stacking of components
  - Embedded actives and passives
  - Polymers
  - Ceramics
  - Enclosures/encapsulants
  - Thermal control features

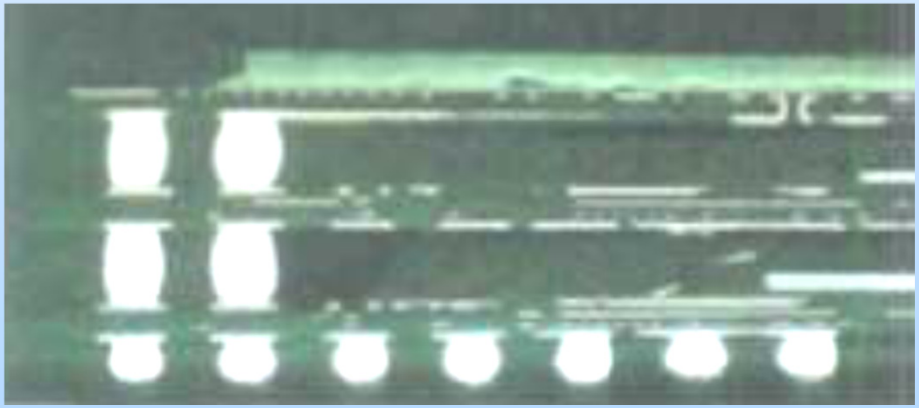


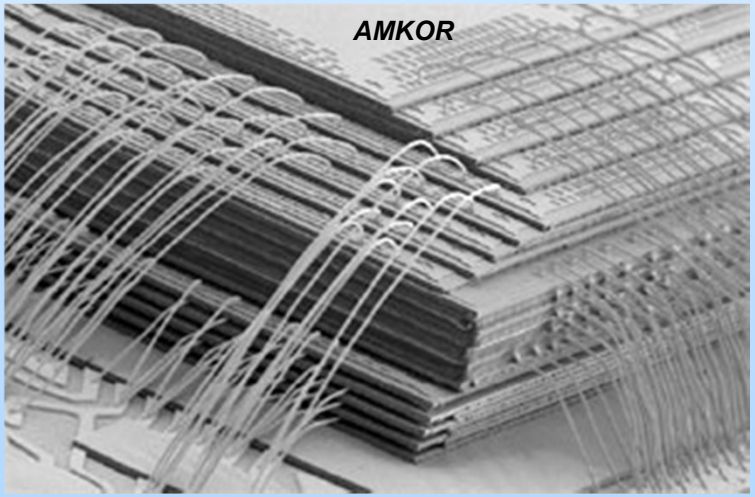
Some Large Device Package Options



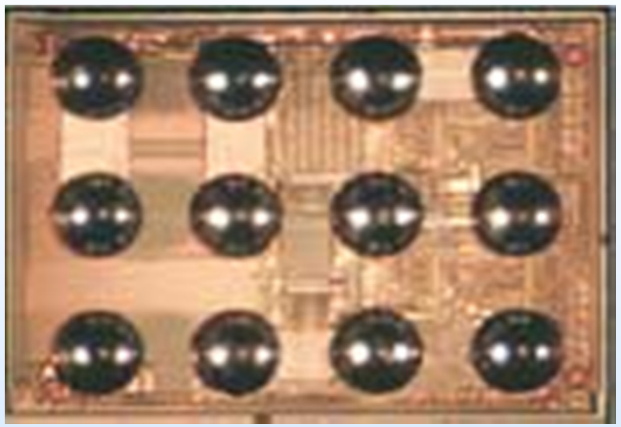


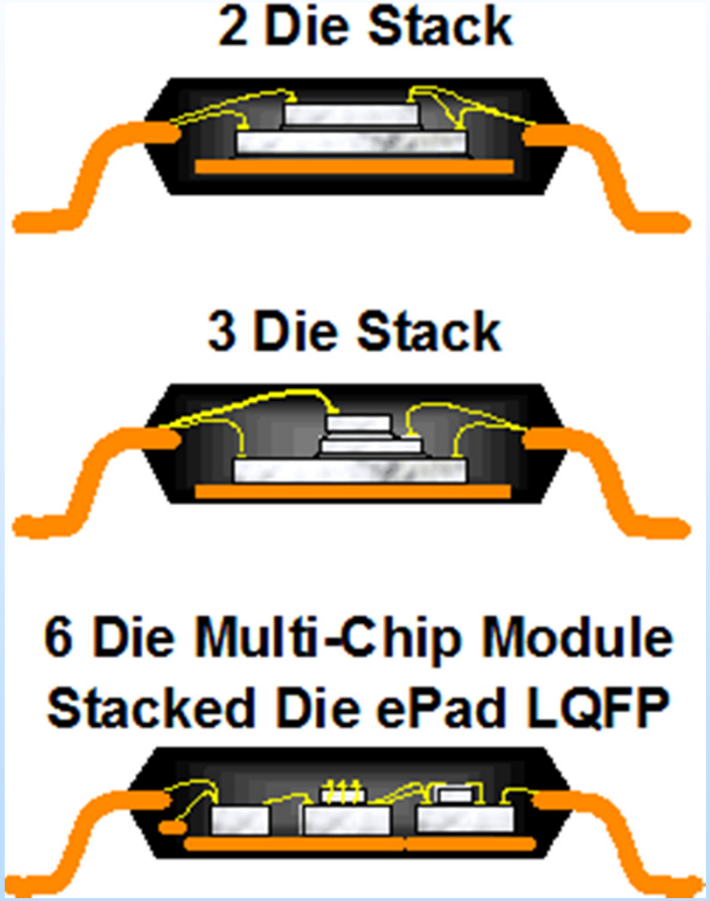
Embedded Capacitor





Some Large Device Package Options





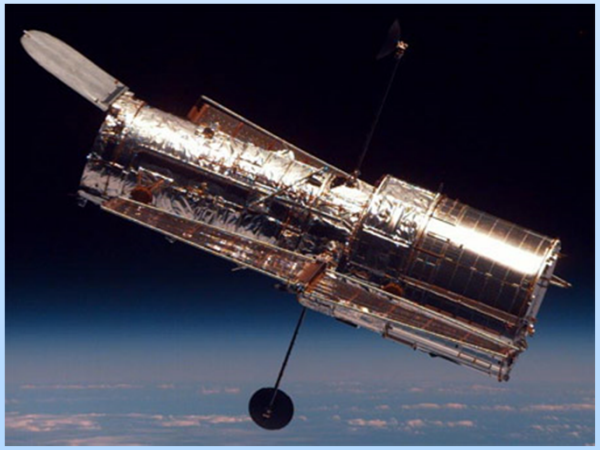
From Amkor's Website http://www.amkor.com/go/packaging

More Complexity is Coming

- Stacking of chips to provide a third dimension of density and complexity
  - Stacking of Field Programmable Gate Arrays (FPGAs) appears imminent
  - Stacking of memory die is “old hat”
  - Through-silicon vias instead of bond wires
    - Maintain speed and allow lots of I/Os
    - High volumetric efficiency
  - Significant manufacturability challenges
    - Material and dimensional interfaces
    - Testability
  - Significant usability challenges
    - Design complexity
    - Handling, testing, rework/replace, risk management
    - Cost versus benefit trades

MIL-PRF-38535, Class Y

- "Y Not" Non-hermetic for Space?
- Proposed new class for M38535, monolithic microcircuits
- Class Y will be for Space level non-hermetic
- Class V will be defined as hermetic only
- Addition to Appendix B, "Space Application"
- Package-specific "integrity" test requirements proposed by manufacturer, approved by DLA* and government space
- The Package Integrity Test Plan must address:
  - Potential materials degradation
  - Interconnect reliability
  - Thermal management
  - Resistance to processing stresses
  - Thermo-mechanical stresses
- G12 Task Group established 01/13/10



* MIL spec qualifying activity Defense Logistics Agency, Land and Maritime

Background

Proposed New Class Y Category

Mike Sampson conceived the idea of a new Class Y for non-Hermetic space parts.

From the San Antonio G-12 Meeting Minutes

The Aerospace Corp. report was presented by Larry Harzstark and David Peters. Mr. Harzstark presentation focused on 2 topics and included:

Class Y Non-hermetic Devices:

Examples of Class Y devices are non-hermetic FPGAs and BGAs. A G12 Task Group was proposed to focus on Class Y devices. At a later meeting the task group was formed. The Task Group Number is 2010-01, the title is Class Y Non-hermetic Device for Space and it is chaired by Shri Agarwal of NASA/JPL.

The Task Group has had two meetings.

Inputs from Class-Y Task Group

Definition of Class Y:

Class Y shall cover those items that are ceramic flip-chip non-hermetic construction and have been subjected to, and passed all applicable requirements of appendix B.

Why do we need the class Y?

Some respondents asked why should space community even allow use of non-hermetic parts. The feasibility of a hermetic ceramic package with underfill flip-chip die has been demonstrated, however, it requires low temperature sealing process as underfill limits the maximum temperature. There are board level concerns as well: increased package stiffness, increased size and weight, poor heat conduction from top of package. There are no current development programs as there is no user interest.

The class Y products are here to stay. The advancements in packaging technology should be covered by the QML system.

Recommend adding the word "hermetic" to the definitions of QML-Q, QML-V products (see next page).

Changes to Appendix-B for class Y:

Most respondents have proposed marking up the existing Appendix-B to reflect changes specific to class Y. The changes will be coordinated with DLA Land & Maritime (formerly DSCC).

MIL-PRF38535 Class Definitions

Ref: MIL-PRF-38535, Rev J

Para 6.4.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic. This product must be assessed by the user to determine if it is appropriate for use in users' application.

Para 6.4.29 Class Q. Items (add,"that are hermetic and") which have been subjected to and passed all applicable requirements of this specification and applicable appendices including qualification testing, screening testing, and TCI/QCI inspections.

(Note: The only known exception would be non-hermetic 5962-9760805(thru 09)QYA 32-bit RISC processors.)

Para 6.4.30 Class V. Items that (add,"are hermetic and") meet all the class Q requirements, and have been subjected to, and passed all applicable requirements of appendix B herein.

Updated Screening Table

MIL-PRF-38535H
TABLE B-2. Class Y Screening Flow

Item	Screen	Test Method and Conditions
Final Part Configuration except the column grid array columns are not attached		
1	Wafer Lot Acceptance	MIL-STD-883 TM 5007
2	Internal Visual Inspection	MIL-STD-883 TM 2010, Test Cond. A, including inspection of bumps
3	CSAM	Manufacturers shall submit their test plan / procedure for approval by QA.
4	Temperature Cycling	MIL-STD-883 TM 1010, Condition C (50 cycles)
5	Constant Acceleration	MIL-STD-883 TM 2001, Condition E (min.) Y_1 orientation only. Manufacturers shall submit justification for approval by QA for reduced test conditions.
6	Visual Inspection	MIL-STD-883 TM 2009
7	Serialization	Laser Marking acceptable
8	Pre Burn-in Electrical Test @ 25°C	Per SMD.
9	Static Burn-in	144 hrs @ 125°C MIL-STD TM 883 1015 Condition B
10	Electrical Parameters (Post Static Burn-in) @ 25°C	Per SMD.
11	Post Static Burn-in Delta Calculation	Per SMD.
12	Dynamic Burn-in	240 hrs at 125°C MIL-STD TM 883 1015 Condition D
13	Electrical Parameters (Post Dynamic Burn-in) @ 25°C	Per SMD.
14	Post Dynamic Burn-in Delta Calculation	Per SMD.
15	Final Percent Defective Allowable (PDA)	MIL-STD-883 TM 5004 PDA includes both Dynamic and Static BI including Delta failures (5% max. overall, 3% max. functional)
16	Final Electrical Test	-55°, +25°, and +125°C, Per SMD.
17	External Visual Inspection	MIL-STD-883, TM 2009
Post-Ball and Column attach (for BGA and CGA Packages)		
18	Solder Ball or Column Attach	Manufacturers shall submit their test plan / procedure for approval by QA.
19	Final Electrical Test	-55°, +25°, and +125°C, Per SMD.
20	Visual Inspection	MIL-STD-883, TM 2009

Updated Screening/QCI Table (Cont'd)

Test	Test Method
Group A	MIL-STD-883, TM5005
Group B	MIL-STD-883, TM5005
Group C	1000 hours 45 (0) or 2000 hours 22 (0) Dynamic Burn-in @ T_A=125C will be performed on each wafer lot for 44,000 device hours per MIL-PRF-38535 B.4.2.c.1.
Group D	Manufacturers are responsible for ensuring the package meets all appropriate Group D tests as defined in MIL-STD 883, TM5005. For Class Y, a packaging integration demonstration test plan shall be submitted to QA for approval. This plan must address potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, and thermo-mechanical stresses. Their plan shall be approved by QA.

Other relevant notes/requirements:

Shelf Life Caution: Because they oxidize when exposed to atmosphere, older columns should be kept in sealed dry packs, which will prevent solder from oxidizing for about 2 years. Storage in dry nitrogen is recommended.

Use of Passive Parts to Enhance Performance of Die: Chip capacitors must be qualified to space level. They should be evaluated in accordance with 38534 Class K element evaluation requirements.

Broad Issues

- 100% Constant Acceleration test vs. die shear/lid torque
- 100% Tri-temp Electrical tests after column attach
- 100% Column attach test/inspection
- Temperature cycle test ramp/dwell time
- Use of capacitors for improved performance
  - Screening and qual requirements have been added to MIL-PRF-38535
- What is a space flight part
  - LGA configuration (yes)
  - CGA configuration (debatable)
- Will the set of 38535 classes, with Class Y added, cover microcircuits for the next several years ? (yes, per the poll taken of major manufacturers)

Future Work

- Refine class-Y definition with DLA Land & Maritime
- Add class-Y to Appendix-B with DLA Land & Maritime
- Update other DLA Land and Maritime documents to add reference to Class Y
- Report on progress status of “hermetic version”
  - Dave Peters, The Aerospace Corporation, to provide updates
- Solder Terminated Microcircuits Investigation as proposed by Boeing (newly formed JC13.2 Task Group)

NEPP Activities

- Continuous surveillance of emerging trends
- Have evaluated embedded passives
  - Partnering with Navy Crane
  - Quite mature technologies, bulk capacitive layer
  - Works but “space” low quantities a challenge
- Have tried to evaluate a novel, flexible, embedded active-die technology
  - Considerable promise
  - Beset by technical problems, particularly die thinning
  - Consider revisiting as technology improves
- Initial evaluations of technical readiness of die thinning, through-hole vias and advance die stacking are needed
- Continue development of Class Y concept